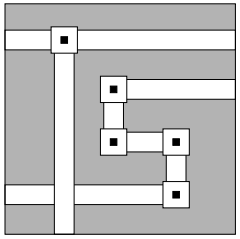

TRILOBYTE SYSTEMS

# The Road Ahead In CPLD & FPGA Design Methodology

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# The Road Ahead for FPGA/CPLD designers…

# …has been paved by ASIC designers!

Standard hardware description languages

- Verilog and VHDL

Simulation

- RTL and gate-level
- Test benches and verification

Synthesis

Static timing analysis

Design style

- Synchronous design
- Hierarchy
- Separate core and IO

Unified design flow

- *Independent* of implementation technology

# Hardware description languages -- PALASM

```
Title    SN54/74S508 MEMORY MAP INTERFACE FOR 8085
Pattern  P7085
Revision A
Author   VINCENT COLI
Company  MMI SUNNYVALE, CALIFORNIA
Date     05/15/82

CHIP SN54/74S508_MEMORY_MAP_INTERFACE_WITH_8085

CLK AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 GND
/OE /E1 ALE I2  I1  I0  /GO E2  E3  VCC

EQUATIONS

GO := /AD3*/AD4*/AD5* AD6*/AD7
    *  E1 * E2 * E3
    *  ALE

/I0 := /AD0

/I1 := /AD1

/I2 := /AD2
```

# Hardware description languages -- Verilog

```
module vince (
  CLK,  AD0,  AD1, AD2, AD3, AD4, AD5,  AD6, AD7,
  OE_L, E1_L, ALE, I2,  I1,  I0,  GO_L, E2,  E3) ;

input CLK, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7,
  OE_L, E1_L, ALE, E2, E3 ;

output I2, I1, I0, GO_L ;

reg I2, I1, I0, GO ;

always @ (posedge CLK)
  GO <= !AD3  && !AD4 && !AD5 &&  AD6 && !AD7
     && !E1_L &&  E2  &&  E3
     &&  ALE ;
assign GO_L = !GO ;

always @ (posedge CLK) I0 <= AD0 ;
always @ (posedge CLK) I1 <= AD1 ;
always @ (posedge CLK) I2 <= AD2 ;

endmodule
```

# Simulation

CPLD and FPGA are no longer used in isolation

You must simulate the entire system

- CPU, memory, ASIC, PLD, CPLD, FPGA, bus

In order to simulate the entire system,

- *all* components must be in the same HDL!

Models of other components are only in Verilog or VHDL, so…

Debugging

- For a reasonably complex design,
  you can no longer debug with "programming and prayer"
- A logic analyzer is not enough when you have buried flops!

Simulate at both RTL and gate-level

## 3 to 5 year design methodology roadmap

## Universal *designers* rather than universal *tools*

Standard HDLs

- Verilog and VHDL

Design entry

- Your favorite text editor
- Maybe use graphical tool (with standard HDL output)

Standard simulation environment

Vendor-specific physical design tools

Standard netlist format

- Verilog and VHDL
- Preserve design hierarchy

Standard timing back-annotation

- SDF
- For static timing analysis (and maybe simulation)